REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-4 are pending in the present application. No claims are amended, cancelled, or added by the present response.

In the outstanding Office Action, Claims 1-3 were rejected under 35 U.S.C. § 102(b) as anticipated by Shokouhi et al. (U.S. Patent No. 6,249,458, herein "Shokouhi"), and Claim 4 was rejected under 35 U.S.C. § 102(b) as anticipated by Javanifard et al. (U.S. Patent No. 5,455,794, herein "Javanifard").

Applicant thanks the Examiner for the courtesy of an interview extended to Applicant's representative on October 11, 2005. During the interview, the differences between the pending claims and the applied art were discussed. The Examiner indicated she would further review the claims in view of a filed response. Arguments similar to those presented during the interview are reiterated below.

The rejection of Claims 1-3 under 35 U.S.C. § 102(b) as anticipated by Shokouhi is respectfully traversed for the following reasons.

Briefly recapitulating, Claim 1 is directed to a semiconductor memory that has a plurality of word lines, a plurality of bit lines, a plurality of memory cells, a Y decoder, and a disconnecting device. Each memory cell is connected to one word line of the plurality of word lines and one bit line of the plurality of bit lines. The Y decoder drives the plurality of bit lines. The disconnecting device is provided to electrically disconnect at least one bit line of the plurality of bit lines from the Y decoder.

In a non-limiting example, Figure 3 shows the semiconductor memory having the plurality of word lines 5 to 8, the plurality of bit lines 3 and 4, the plurality of memory cells 9 to 16, the Y decoder 1, and the disconnecting device 17.

Turning to the applied art, Shokouhi shows in Figure 3 a memory device having a decoder 850 connected through switches 840 to a plurality of bit lines BL0 to BLX. However, Shokouhi fails to teach or suggest that the switches 840 are electrically disconnecting at least one bit line of lines BLO-BLX. The outstanding Office Action relies on the disclosure of Shokouhi at column 4, lines 61-63, for asserting that the switch 840 operate "in a manner similar to switches 830," which Shokouhi discloses as electrically disconnecting a bit line. However, Applicant respectfully submits that the switches 830 shown in Figure 3 of Shokouhi disconnect the bit lines BLO-BLX based on a BLL signal but the BLL signal is not provided to switch 840.

Therefore, Applicant respectfully submits that switch 840 does not perform the same operation as the switches 830 as asserted in the outstanding Office Action at page 3, lines 14-16. Further, an element corresponding to the switch 840 is a switch 820, and there is no portion in the source-side that corresponds to the switch 830 disconnecting the bit lines.

Accordingly, it is respectfully submitted that Claim 1 and each of the claims depending therefrom patentably distinguish over Shokouhi.

Regarding the rejection of Claim 4 under 35 U.S.C. § 102(b) as anticipated by Javanifard, that rejection is respectfully traversed for the following reasons.

The outstanding Office Action relies on Figures 2 and 3 of Javanifard for showing various claimed elements and combines the teachings of Figures 2 and 3 as described in the first full paragraph on page 5 of the outstanding Office Action. Applicant respectfully

submits that a rejection under 35 U.S.C. § 102 is improper when distinct embodiments of a same reference are combined.

However, assuming arguendo that the combination of the two different embodiments shown respectively in Figures 2 and 3 of Javanifard is proper, Applicant respectfully submits that Javanifard specifically discloses at column 5, lines 56-64, that

> [a]lthough the circuit of FIG. **2** allows the use of internal charge pumps to generate voltages for programming and erasing a flash EEPROM memory array, it does not allow the use of an external source of power. FIG. **3** is a block diagram illustrating a circuit arrangement **30** designed in accordance with the present invention which allows switching between an external source and internal charge pumps in order to provide source voltage to operate a flash EEPROM memory array [underlined added].

Thus, Javanifard specifically states that Figure 2 does not allow "an **external source** of power" while the embodiment shown in Figure 3 "allows switching between **an external source** and internal charge pumps in order to provide source voltage to operate a flash EEPROM memory array" (emphasis added).

Therefore, as discussed during the interview, Applicant respectfully submits that Javanifard discloses two embodiments which are not compatible with each other. Thus, the combination of these two embodiments suggested by the outstanding Office Action in the first full paragraph on page 5 appears to be improper even under 35 U.S.C. § 103(a).

For the above noted reasons, Applicant respectfully submits that Claim 4 patentably distinguishes over Javanifard.

Consequently, in light of the above discussion, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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